National Semiconductor

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LM5073
100V Power Over Ethernet PD Interface with Aux Support

General Description

The LM5073 Powered Device (PD) interface provides a high performance solution that is fully compliant to IEEE 802.3af for a PD connecting into Power over Ethernet (PoE) networks. The LM5073 provides the flexibility for the PD to also accept power from unregulated auxiliary sources such as AC adapters and solar cells in a variety of configurations. The low $R_{DS(ON)}$ PD interface hot swap MOSFET and programmable DC current limit extend the range of LM5073 applications up to twice the power level of IEEE 802.3af compliant devices. The 100V maximum voltage rating simplifies selection of the transient voltage suppressor that protects the PD from network transients. Control outputs for a separate DC-DC converter are provided to allow freedom to select the best DC-DC converter topology for the particular application.

Features

PD Interface

- Fully Compliant IEEE 802.3af PD Interface
- Versatile Auxiliary Power Options
- 13V Minimum Front Auxiliary Power Range
- 9V Minimum Rear Auxiliary Power Range
- Programmable DC Current Limit up to 800 mA
- 100V, 0.7Ω Hot Swap MOSFET
- Integrated PD Signature Resistor
- Integrated PoE Input UVLO
- Inrush Current Limit
- PD Classification Capability
- Thermal Shutdown Protection
- Line Over Voltage Protection
- Complementary Open Drain Outputs for Controlling a DC-DC Converter
- Power Good Indicator

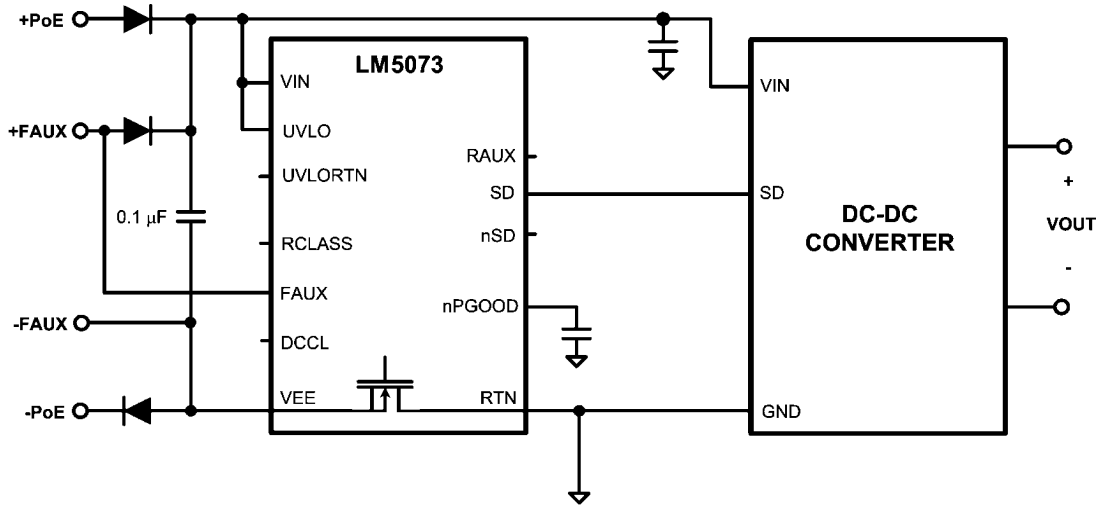
Applications

- IEEE 802.3af Compliant PoE Powered Devices
- Non-Compliant, Application Specific Devices
- Higher Power Ethernet Powered Devices

Packages

- TSSOP-14 EP (Exposed Pad)

Simplified Application Diagram



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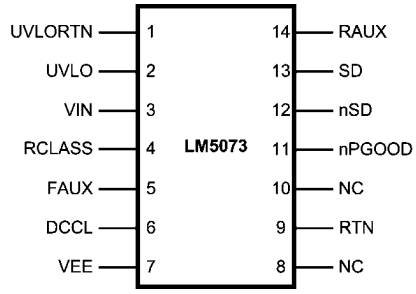
Connection Diagram



14 Lead TSSOP-EP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5073MH	TSSOP-14EP	MXA14A	94 Units per Rail
LM5073MHX	TSSOP-14EP	MXA14A	2500 Units on Tape and Reel

Pin Descriptions

Pin Number	Name	Description
1	UVLORTN	Return for the external UVLO programming resistor divider.
2	UVLO	Line under-voltage lockout programming pin.
3	VIN	Positive supply pin for the PD interface and the DC-DC converter interface.
4	RCLASS	PD Classification programming pin.
5	FAUX	Front auxiliary power enable pin.
6	DCCL	PD interface DC current limit programming pin.
7	VEE	Negative supply pin for the PD interface; connected to PoE and/or front auxiliary power return path.
8	NC	No internal connection.
9	RTN	DC-DC converter power return; connected to the drain of the internal PD interface hot swap MOSFET.
10	NC	No internal connection.
11	nPGOOD	PD interface power good delay and indicator. nPGOOD is low when the hot swap MOSFET drain to source voltage is less than 1.5V.
12	nSD	Open drain, active low shut down signal to the DC-DC converter. The nSD pin switches to the high impedance state when nPGOOD is less than 2.5V.
13	SD	Open drain, active high shut down signal to the DC-DC converter. The SD pin switches to the low state when nPGOOD is less than 2.5V.
14	RAUX	Rear auxiliary power enable pin, and dominant/non-dominant selection.
	EP	Exposed metal pad on the underside of the device. It is recommended to connect this pad to a PC Board plane connected to the VEE pin to improve heat dissipation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN, FAUX, UVLO, RTN to VEE (Note 6)	-0.3V to 100V
UVLORTN to VEE	-0.3V to 16V
DCCL, RCLASS to VEE	-0.3V to 7V
nPGOOD, nSD, SD to RTN	-0.3V to 16V
RAUX to RTN	-0.3V to 100V
ESD Rating	
Human Body Model (Note 2)	2000V
Lead Soldering Temp. (Note 3)	
Wave (4 seconds)	260°C
Infrared (10 seconds)	240°C
Vapor Phase (75 seconds)	219°C
Storage Temperature	-55°C to 150°C
Junction Temperature	150°C

Operating Ratings

V_{IN} voltage	9V to 70V
Operating Junction Temperature	-40°C to 125°C

Electrical Characteristics (Note 4)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 48V unless otherwise indicated. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
	VIN Supply Current	Normal Operation		2	**3**	mA
Detection and Classification						
	VIN Signature Startup Voltage				**1.5**	V
	Signature Resistance		**23.25**	24.5	**26**	kΩ
	Signature Resistor Disengage / Classification Engage	V_{IN} Rising	**11.0**	12	**12.8**	V
	Hysteresis			1.9		V
	Classification Current Turn Off	V_{IN} Rising	**22**	23.5	**25**	V
	RCLASS Voltage		**1.213**	1.25	**1.287**	V
	Supply Current During Classification	V_{IN} = 17V		0.7	**1.1**	mA
Line Under Voltage Lock-Out						
	Default UVLO Release	V_{IN} Rising	**36**	38.5	**40**	V
	Default UVLO Lock out	V_{IN} Falling	**29.5**	31	**32.5**	V
	Default UVLO Hysteresis		**6**			V
	Programmed UVLO Reference Voltage	V_{IN} > 12.5V	**1.2**	1.24	**1.28**	V
	Programmed UVLO Hysteresis Current	V_{IN} > UVLO	**16**	20	**24**	µA
	UVLORTN Pull Down Resistance	V_{IN} > 12.5V		55	**150**	Ω
	UVLO Filter			300		µs
Power Good						
	VDS Required for Power Good Status		**1.3**	1.5	**1.7**	V
	VDS Hysteresis of Power Good Status		**0.8**	1	**1.2**	V
	VGS Required for Power Good Status		**4.5**	5.5	**6.5**	V
	Default Delay Time of Loss-of Power Good Status			30		µs
	nPGOOD Current Source		**40**	55	**70**	µA
	nPGOOD Open circuit Voltage		**3.5**	4	**5.5**	V
	nPGOOD Pull Down Resistance			180	**300**	Ω
	nPGOOD Threshold		**2**	2.5	**3**	V
Shutdown Outputs						
	nSD/SD Pull Down Resistance			180	**300**	Ω
	Leakage	nSD/SD = 16V			**1**	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Hot Swap						
RDS(ON)	Hot Swap MOSFET Resistance			0.7	**1.5**	Ω
	Hot Swap MOSFET Leakage				**100**	µA
	Inrush Current Limit	V_{DS} = 4.0V	**120**	150	**180**	mA
	Default DC Current Limit	V_{DS} = 4.0V	**380**	440	**510**	mA
	High DC Current Limit	V_{DS} = 4.0V	**690**	800	**930**	mA
	Current Limit Programming Accuracy	V_{DS} = 4.0V	**-12**		**12**	%
Hot Swap Over-Voltage Protection						
	VIN OVP Threshold		**60**	65	**70**	V
	VIN OVP Threshold, Hysteresis			3		V
Auxiliary Power Option						
	FAUX Threshold		**8.1**	8.7	**9.5**	V
	FAUX Hysteresis			0.5		V
	FAUX Pull Down Current			50		µA
	RAUX Lower Threshold (I = 22 µA)	RAUX Pin Rising	**2.3**	2.7	**3.4**	V
	RAUX Lower Threshold Hysteresis			0.8		V
	RAUX Upper Threshold (I = 250 µA)	RAUX Pin Rising	**5.4**	6.2	**7.4**	V
	RAUX Lower Threshold Current		**14**	22	**30**	µA
	RAUX Upper Threshold Current		**170**	250	**330**	µA
PDI Thermal Shutdown (Note 5)						
	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	MXA Package		40		°C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 3: For detailed information on soldering the plastic TSSOP package, refer to the Packaging Databook available from National Semiconductor.

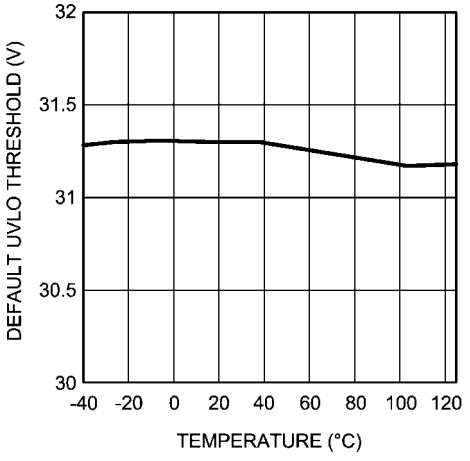
Note 4: Minimum and Maximum limits are guaranteed through test, design, or statistical correlation using Statistical Quality Control (SQC) methods. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purpose only. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: Device thermal limitations may limit usable range.

Note 6: During rear auxiliary operation, the RTN pin can be approximately -0.4V with respect to VEE. This is caused by normal internal bias currents, and will not harm the device. Application of external voltage or current must not cause the absolute maximum rating to be exceeded.

Typical Performance Characteristics

Default UVLO Threshold vs Temperature



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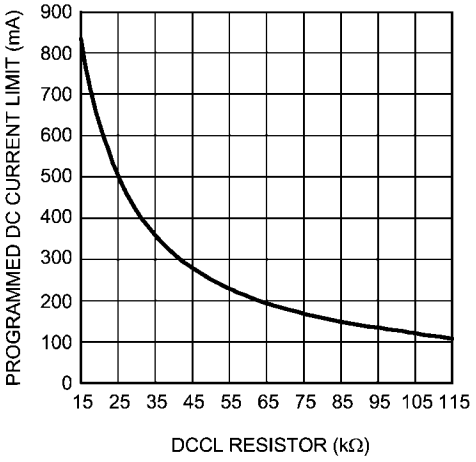
DC Current Limit vs. DCCL Resistor



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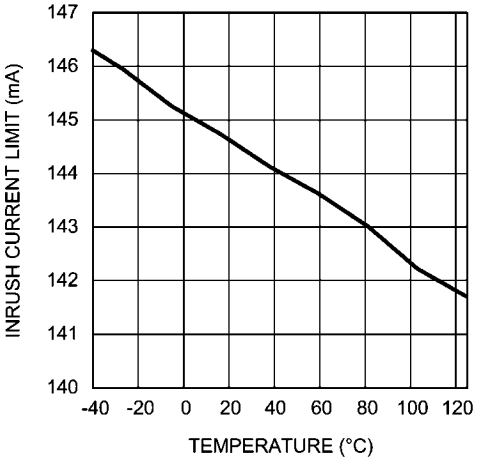
Inrush Current Limit vs Temperature



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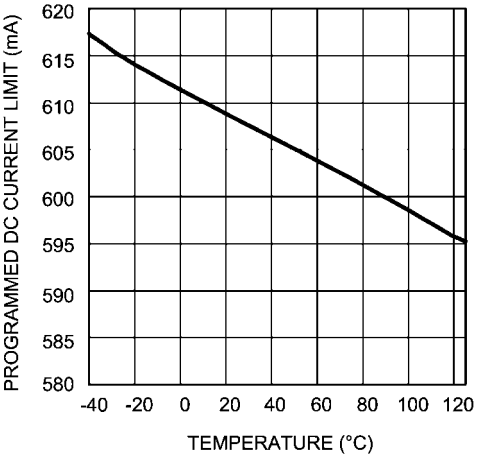
Programmed DC Current Limit vs Temperature



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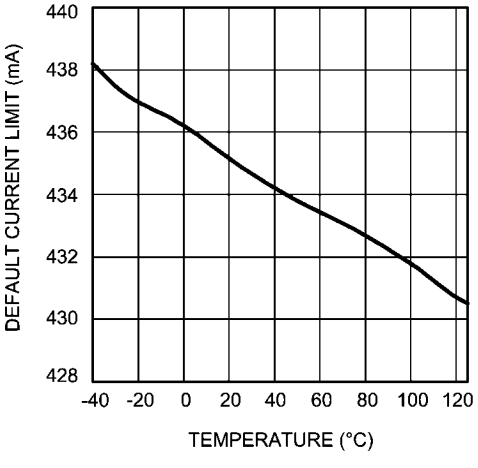
Default DC Current Limit vs Temperature



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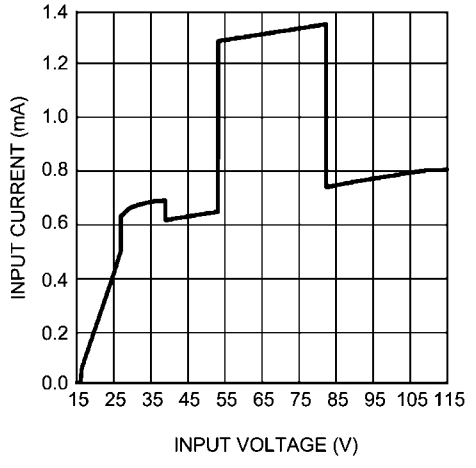
Input Current vs Input Voltage



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Block Diagram

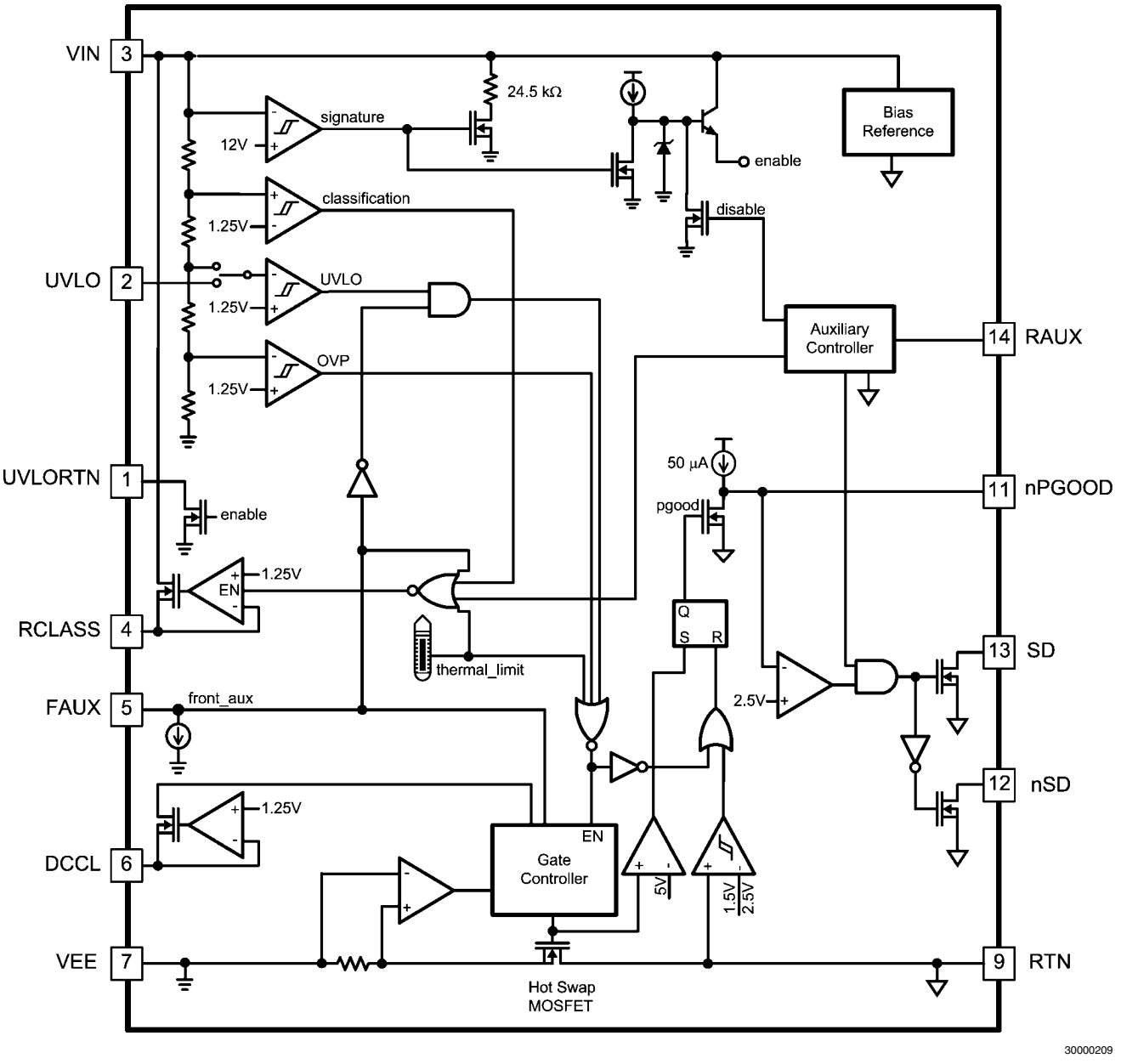


FIGURE 1. LM5073 Top Level Block Diagram

Description of Operation and Applications Information

The LM5073 integrates a fully IEEE 802.3af compliant PD interface with versatile auxiliary power support. When combined with a separate DC-DC converter, it provides a complete power solution for Powered Devices (PD) that connect to PoE systems.

The LM5073 provides the following features:

1. The input voltage rating up to 100V allows greater flexibility when selecting a transient surge suppressor to protect the PD from voltage transients encountered in PoE applications.
2. The integration of the PD signature resistor, inrush current limit, programmable input voltage under-voltage lock-out (UVLO), PD classification, and thermal shutdown simplifies PD implementation.
3. The PD interface accepts power from auxiliary sources including AC adapters and solar cells in various configurations over a wide range of input voltages. Auxiliary power input can be programmed to be either non-dominant or dominant over PoE power.
4. Programmable DC current limit to support PD applications requiring input currents up to 800 mA.
5. Complementary open drain outputs for controlling a DC-DC converter.

6. A power good flag pin allows an accurate power good delay to be programmed and provides the option of driving a power good indicator LED.
7. Input line over voltage protection for downstream circuits, including the DC-DC converter.

DC-DC Converter Selection

A PD designed with LM5073 can be optimized for a variety of applications by selecting the DC-DC converter from a wide range of topologies. Topology selection enables several design trade-offs including efficiency, complexity, and cost.

For example, the LM5025 controller for the Active Clamp Forward topology can be paired with the LM5073 for increased efficiency, especially at higher power levels. In cases where isolation is not required an LM5576 regulator with a built in buck switch provides a simple, low cost solution.

The 100V capability of the LM5073 protects against input voltage transients, especially in the case of a hot swapping front auxiliary power. The LM5073 has built-in over-voltage protection such that a DC-DC converter with input voltage rating as low as 65V can be safely used.

The DC-DC converter must have a soft start feature to control the input current during startup. The soft-start process reduces the surge of inrush current and eliminates any tendency of the output voltage to overshoot during startup. The converter should be started slowly enough such that the input current does not exceed the PD interface hot swap MOSFET DC current limit or the current limit of the PSE, otherwise the PD will not start correctly.

Modes of Operation

Per the IEEE 802.3af specification, when a PD is connected to a PoE system it transitions through several operating modes in sequence including detection, classification (optional), turn-on inrush, and normal DC operation. Each operating mode corresponds to a specific voltage range supplied from the PSE. *Figure 2* shows the IEEE 802.3af specified sequence of operating modes and the corresponding PD input voltages at the RJ-45 connector.

Current steering diode bridges are required for the PD interface to accept all allowable connections and polarities of PoE voltage from the RJ-45 connector (see the example application circuit in *Figure 11*). The bridge voltage drop will reduce the input voltage sensed by the LM5073. To guarantee full compliance to the specification in all operating modes, the LM5073 takes into account the voltage drop across the bridge diodes and responds appropriately to the voltage received from the PoE cable. *Table 1* presents the response in each operating mode to voltages at the PD input connector and between the VIN and VEE pins.

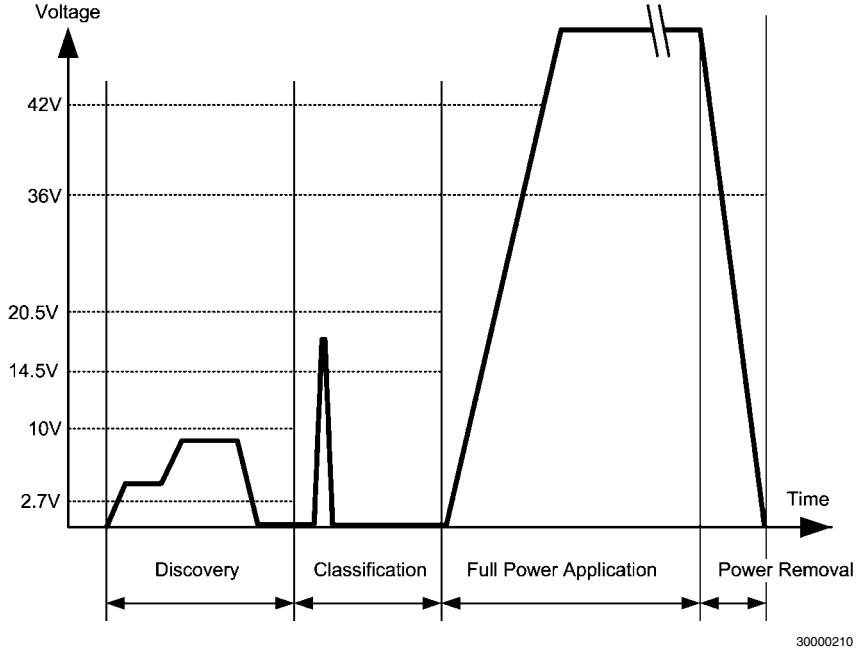


FIGURE 2. Sequence of PoE Operating Modes

TABLE 1. Operating Modes With Respect To Input Voltage

Mode of Operation	Voltage at PD Input Connector per IEEE 802.3af	LM5073 Input Voltage (VIN pin to VEE pin)
Detection (Signature)	2.7V to 10.1V	1.5V to 10.0V
Classification	14.5V to 20.5V	12V to 23.5V
Startup Threshold	42V max	38V (UVLO Release, VIN Rising)
Normal Operation	36V to 57V	65V to 32V (UVLO, VIN Falling)

Detection Signature

In the detection mode, a PD must present a signature resistance between 23.75 kΩ and 26.25 kΩ to the PoE power sourcing equipment. This signature impedance distinguishes the PD from non-PoE equipment to protect the latter from being accidentally damaged by inadvertent application of PoE voltage levels. To simplify the circuit implementation, the LM5073 integrates the signature resistor, as shown in *Figure 3*.

During the detection mode, the voltage across the VIN and VEE pins is less than 10V. Once detection mode is complete, the LM5073 will disengage the signature resistor to reduce power loss in all other modes.

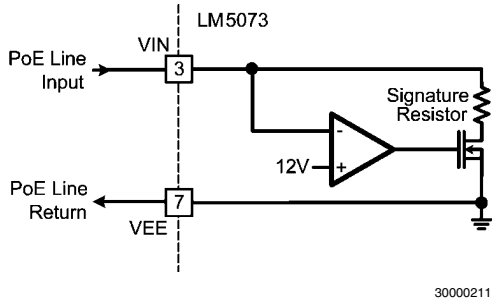


FIGURE 3. Detection Circuit With Integrated PD Signature Resistor

Classification

Classification is an optional feature of the IEEE 802.3af specification. It is primarily used to identify the power requirements of a particular PD. This feature will allow the PSE to allocate the appropriate available power to each device on the network. Classification is performed by measuring the current flowing into the PD during this mode. IEEE 802.3af specifies five power classes, each corresponding to a unique range of classification current, as presented in *Table 2*. As shown in *Figure 4*, the LM5073 simplifies the classification implementation by requiring a single external resistor connected between the RCLASS and VEE pins to program the classification current. The resistor value required for each class is also given in *Table 2*.

During the classification mode, the voltage between the VIN and VEE pins is between 12V and 23.5V. In this voltage range, the class resistor R_{CLASS} is engaged by enabling the 1.25V buffer amplifier and MOSFET. After classification is complete, the voltage from the PSE will increase to the normal operating voltage of the PoE system (48V nominal). When VIN rises above 23.5V, the LM5073 will disengage the RCLASS resistor to reduce on-chip power dissipation.

The classification feature is disabled when either the front or rear auxiliary power options are selected, as the classification function is not required when power is supplied from an auxiliary source. The classification function is also disabled when the LM5073 reaches the thermal shutdown temperature threshold (nominally 165°C). This may occur if the LM5073 is operated at elevated ambient temperatures and the classification time exceeds the IEEE 802.3af limit of 75 ms.

When the classification option is not required, simply leave the RCLASS pin open to set the PD to the default Class 0 state. Class 0 requires that the PSE allocate the maximum IEEE 802.3af specified power of 15.4W (12.95W at the PD input terminals) to the PD.

TABLE 2. Classification Levels and Required External Resistor Value

Class	PD Max Power Level		I_{CLASS} Range		LM5073 R_{CLASS} Value
	From	To	From	To	
0 (Default)	0.44W	12.95W	0 mA	4 mA	Open
1	0.44W	3.84W	9 mA	12 mA	130Ω
2	3.84W	6.49W	17 mA	20 mA	71.5Ω
3	6.49W	12.95W	26 mA	30 mA	46.4Ω
4	Reserved	Reserved	36 mA	44 mA	31.6Ω

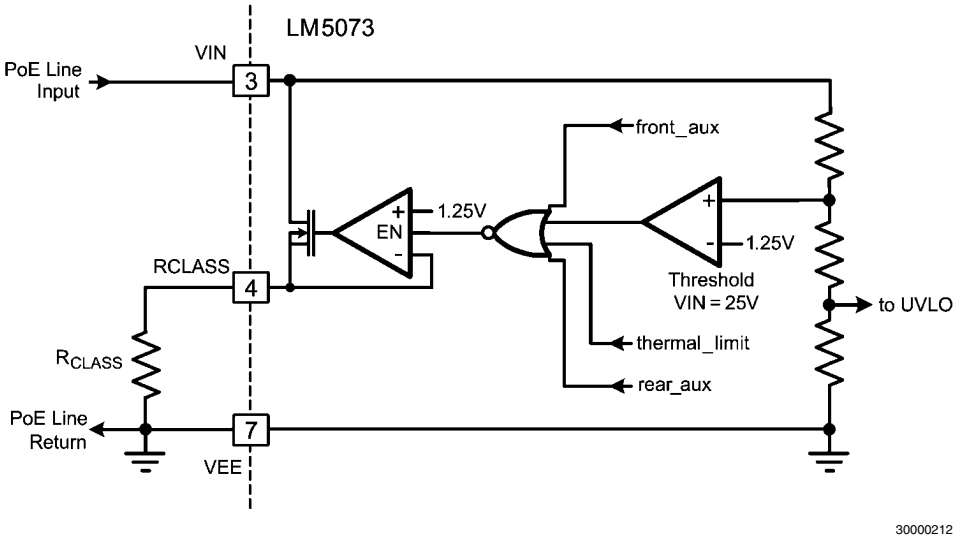


FIGURE 4. PD Classification – Fulfilled With a Single External Resistor

Undervoltage Lockout (UVLO)

The LM5073 contains both programmable and default input Under Voltage Lock Out (UVLO) circuits. *Figure 5* illustrates the block diagram of the LM5073 UVLO circuit. When the UVLO pin is connected to the VIN pin the internal default thresholds and hysteresis are selected, requiring no external components to comply with the IEEE 802.3af UVLO specifications. To program the UVLO threshold and hysteresis to custom values, use two external resistors R1 and R2. Connecting an external resistor divider to the UVLO pin automatically overrides the default UVLO settings.

The LM5073's UVLO circuit continuously monitors the PoE input voltage between the VIN and VEE pins. When the VIN voltage rises above the upper threshold, either default or programmed, the UVLO circuit will enable the hot swap MOSFET and initiate the startup inrush sequence. During normal operating mode, when the VIN voltage falls below the default or the programmed lower threshold, the LM5073 disables the PD by disabling the hot swap MOSFET. A built-in 300 µs timer delays the disable signal, to prevent disabling the hot swap MOSFET during intermittent transients.

The UVLO thresholds are determined by the following considerations. The PD can draw a maximum current of 400 mA during IEEE 802.3af PoE operation. This current will cause a voltage drop of up to 8V over a 100m long Ethernet cable. The PD front-end current steering diode bridges may introduce an additional 2V drop. To guarantee successful startup at the minimum PoE voltage of 42V and to continue operation at the minimum requirement of 36V, as specified by IEEE 802.3af, these voltage drops must be taken into account. Accordingly, the LM5073 UVLO default thresholds are set to 38V, on the rising edge of VIN, and 31V on the falling edge of VIN. The 7V nominal hysteresis of the default UVLO function, along with the inrush current limit (discussed in the next section), prevents false starts and chattering during startup.

In addition to the default settings, the UVLO threshold and hyteresis can be programmed independently to custom values. After selecting R1 to program the UVLO hysteresis, the ratio between R1 and R2 determines the UVLO threshold. The resistors should be selected to satisfy the following relationships:

$$R1 = V_{HYS} / 20\ \mu A$$

$$R2 = \frac{1.25V \times R1}{V_{UVLO}}$$

Where V_{UVLO} is the upper (positive going) trip point and V_{HYS} is the difference betweeen the upper and lower trip points.

The UVLO thresholds should not be programmed below the classification threshold or above the OVP threshold.

The UVLO signal will be overridden by the front auxiliary power option (see details in the FAUX section).

The UVLO function can also be used to implement a remote enable / disable function. Pulling the UVLO pin down below the UVLO threshold disables the interface and the control outputs for the DC-DC converter.

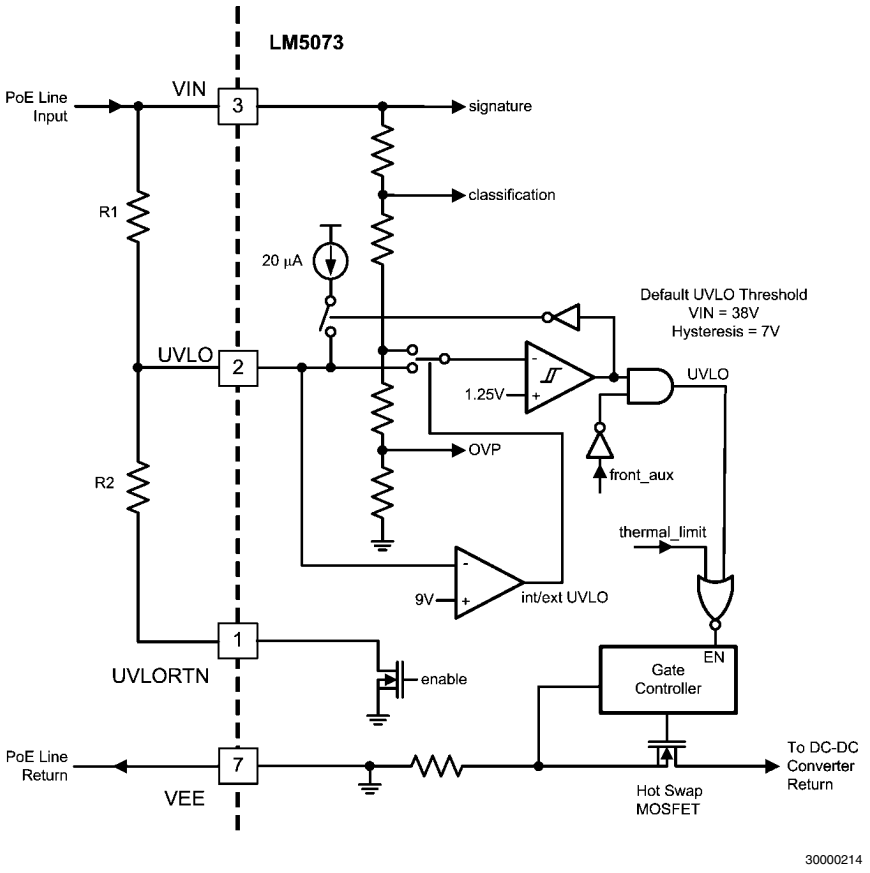


FIGURE 5. Programmable and Default Input UVLO Functions

Over-Voltage Protection

To protect the downstream DC-DC converter from excessive voltage, the hot swap MOSFET is disabled when the 65V (nominal) over-voltage protection (OVP) threshold is exceeded. This allows the 100V rated LM5073 to work safely with a lower voltage rated DC-DC converter. The SD and nSD signals which enable the DC-DC converter are delayed by the power good filter as shown in *Figure 7*. The DC-DC converter will continue to operate through a short duration UVLO condition provided the power good filter does not expire and sufficient voltage remains at the input to the DC-DC converter. When the input voltage returns to normal, the hot swap MOSFET is re-enabled. Once the voltage between RTN and VEE is below 1.5V, power good will be re-asserted.

Inrush Current Limit

Inrush current limit is required to control the charging of the DC-DC converter input capacitors when power is first applied. This reduces stress on components and prevents startup oscillations that would occur if unlimited current were drawn from the PoE network.

According to IEEE 802.3af, the input capacitance of the PD power supply must be at least 5 µF (between the VIN and RTN pins). Considering the capacitor tolerance and the effects of voltage and temperature, a nominal capacitor value of at least 10 µF is recommended. The input capacitors remain discharged during detection and classification modes of the PD interface. The hot swap MOSFET is turned on when the voltage between the VIN and VEE pins rises above the UVLO release threshold. When enabled, the hot swap MOSFET delivers a regulated inrush current of 150 mA to charge the input capacitors of the DC-DC converter.

The inrush current causes a voltage drop along the PoE Ethernet cable (20Ω maximum) that reduces the input voltage sensed by the LM5073. To avoid erratic turn-on (hiccups), the UVLO hysteresis must be greater than the input voltage drop due to cable resistance. If the 7V default hysteresis is insufficient, it should be programmed to a higher value.

DC Current Limit Programming

The LM5073 provides a default DC current limit of 440 mA nominal. This default limit is selected by leaving the DCCL pin open.

The LM5073 allows the DC current limit to be programmed within the range of 150 mA to 800 mA. *Figure 6* shows the method to program the DC current limit with an external resistor, R_{DCCL}. The relationship between the R_{DCCL} value and the DC current limit, I_{DC}, satisfies the following equation:

$$R_{DCCL}\ (k\Omega) = \frac{100\ mA}{I_{DC}\ (mA)} \times 127\ k\Omega$$

The maximum recommended DC current limit is 800 mA. While thermal analysis should be a standard part of any power supply design, it may warrant additional attention if the DC current limit is programmed to values in excess of 440 mA.

The analysis should include evaluations of the dissipation capability of LM5073 package, heat sinking properties of the PC board, ambient temperature, and other heat dissipation factors of the operating environment.

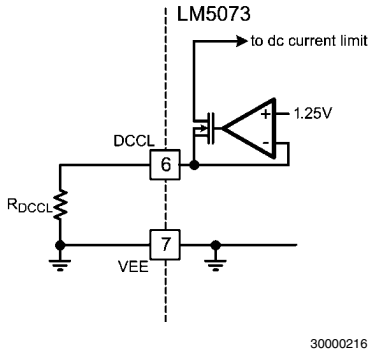


FIGURE 6. Input DC Current Limit Programming via R_{DCCL}

Power Good Operation

The nPGOOD pin serves as a power good flag. It can be used with a delay timing capacitor to delay the assertion of the shutdown pins. It can also be used to drive an optional 'powered from PoE' indicator. The voltage on the nPGOOD pin controls the shutdown pins used to enable the DC-DC converter. An internal 50 µA pull-up current source will pull the nPGOOD pin up to about 4V. External loads (such as an LED) may pull the output up to a maximum of 16V.

The power good status indicates that the input capacitors of the DC-DC converter are fully charged through the hot swap MOSFET and the circuit is ready for the DC-DC converter to start up. The power good status is issued by pulling down the nPGOOD pin to a logic low level relative to the RTN pin.

Once the power good status is established, the nPGOOD pin voltage will be pulled down quickly, and the two DC-DC converter control outputs, SD and nSD, will change states. When the nPGOOD pin is low, the SD pin is active low and the nSD pin is high impedance.

The nPGOOD pin can be configured to perform multiple functions. As shown in *Figure 7*, it can be used to implement a "Powered from PoE" indicator using an LED with a series current limiting resistor connected to a positive supply less than 16V. This is useful when the auxiliary power source is directly connected to the input of the DC-DC converter stage, a situation known as rear auxiliary power (see Auxiliary Power Options below). In such a configuration, the nPGOOD pin will illuminate the LED when the PD is operating from PoE power but not when it is powered from the auxiliary source. The "Powered from PoE" indicator is not applicable in systems implementing the front auxiliary power configuration (see Auxiliary Power Options below) because both PoE and auxiliary supply current pass through the hot swap MOSFET. In this configuration, the nPGOOD pin is active when either PoE power or auxiliary power is applied.

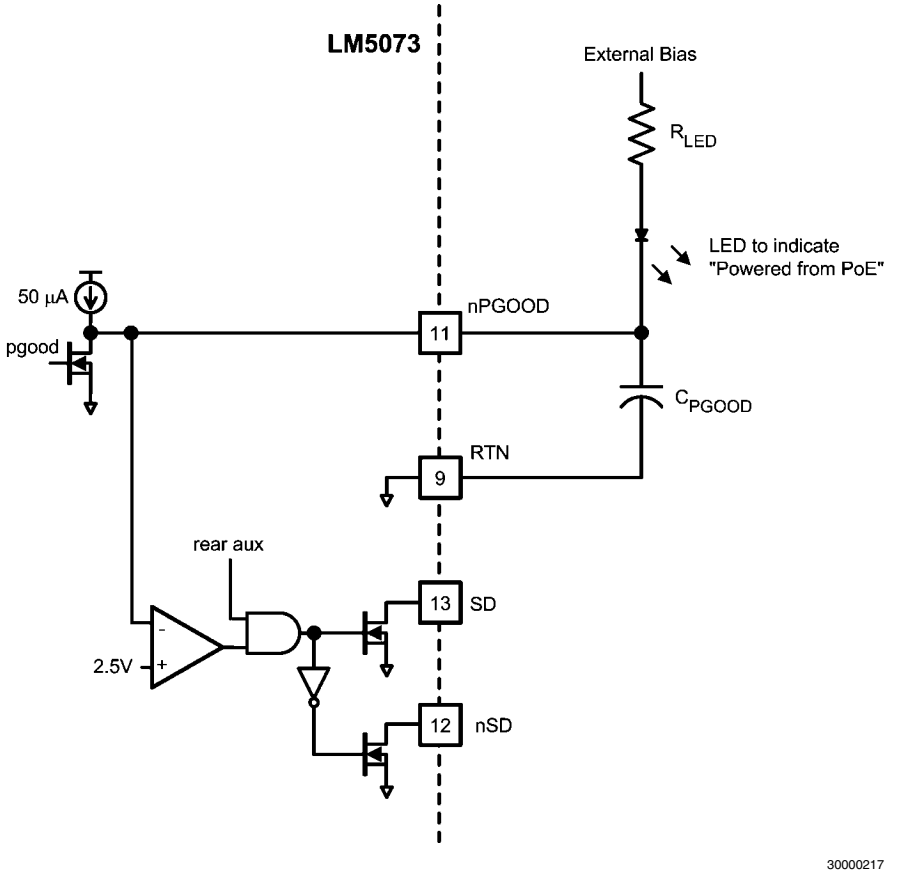


FIGURE 7. "Powered-from-PoE" Indictor, Power Good Delay Timer and Shut Down Control Outputs

The nPGOOD pin can also be used to implement a delay timer by adding a capacitor from the nPGOOD pin to the RTN pin. This delay timer will prevent the interruption of the DC-DC converter's operation in the event of an intermittent loss of power good status. This can be caused by PoE line voltage transients that may occur when switching between normal PoE power and a backup supply (e.g. a battery or UPS). Such a condition will create a new "hot swap" event if the backup supply voltage is greater than the PoE supply. Since the hot swap MOSFET will likely limit current during such a sudden input voltage change, the nPGOOD pin will momentarily switch to the high state. A capacitor on this pin will delay the transition of the nPGOOD pin to provide continuous operation of the DC-DC converter during such transients. The power good filter delay time and capacitor value can be selected with the following equation:

$$C_{PGOOD}\ (nF) = 20 \times t_{PG\_DELAY}\ (ms)$$

For example, selecting 100 nF for C_{PGOOD}, the delay time will be 5 ms. The delay required for continuous operation will depend on the amplitude of the transient, the DC current limit, the load, and the total amount of input capacitance. The nPGOOD delay timer will not guarantee continuous operation if the hot swap MOSFET is in current limit for an extended period, causing a thermal limit condition. This will result in a complete shutdown of the DC-DC converter, though no elements in the system will be permanently damaged and normal operation will resume momentarily.

The power good status also affects the default DC current limit. Should the sensed drain to source voltage of the hot swap MOSFET (from RTN to VEE) exceed 2.5V, the LM5073 will increase the DC current limit from the default 440 mA to 800 mA (High DCCL). This higher current limit will speed recovery from an input voltage downward step, allowing continued operation of the PD. This higher current limit will remain in effect until one of the following events occurs: (i) the power good status is lost for longer than t_{PG_Delay}, at which time the DC-DC converter will be disabled, (ii) the increased power dissipation in the hot swap MOSFET causes a thermal limit condition as previously discussed, or (iii) the hot swap MOSFET drain to source voltage falls below 1.5V to re-establish power good status. Note that if the DC current limit has been programmed externally with R_{DCCL} (see the DC current limit section), then the DC current limit will remain at the programmed level even when the power good status is lost.

Enabling the External DC-DC Converter

The LM5073 has complementary active high (SD) and active low (nSD) shut down outputs that can be used with any DC-DC converter that has an enable input. When nPGOOD pin is low (< 2.5V), the SD pin will be in the low state and the nSD pin will be high impedance. In cases where the pull up internal to the DC-DC converter is weak, an additional pull-up may be desirable for better noise immunity. Alternatively, the nSD output may be connected to the UVLO or Soft Start pins of the DC-DC converter when a dedicated enable input is not available. The open drain output will not interfere with normal operation of the DC-DC converter's UVLO or Soft-Start.

The external pull-ups for the SD or nSD pins must limit the voltage at each pin to no more than 16V relative to RTN, and limit the sink current to 1 mA or less.

Auxiliary Power Options

The LM5073 allows the PD to receive power from auxiliary sources like AC adapters and solar cells in addition to the PoE enabled network. This is a desirable feature when the total system power requirements exceed the PSE's load capacity. Furthermore, with the auxiliary power option, the PD can be used in a standard Ethernet (non-PoE) system.

For maximum versatility, the LM5073 accepts two different auxiliary power configurations. The first one, shown in *Figure 8*, is the front auxiliary (FAUX) configuration in which the auxiliary source is "diode OR'd" with the voltage available from the Ethernet connector. The second configuration, shown in *Figure 9*, is the rear auxiliary (RAUX) option in which the auxiliary power bypasses the PoE interface altogether and is connected directly to the input of the DC-DC converter through a diode. The FAUX option is desirable if the auxiliary power voltage is similar to the PoE input voltage. However, when the auxiliary supply voltage is much lower than the PoE input voltage, the RAUX option is more favorable because the current from the auxiliary supply is not limited by the hot swap MOSFET DC current limit. A comparison of the FAUX and RAUX options is presented in *Table 3*. Note the FAUX and RAUX pins are not reverse voltage protected. If the polarity of the auxiliary supply is not guaranteed, then a series blocking diode should be added for reverse polarity protection.

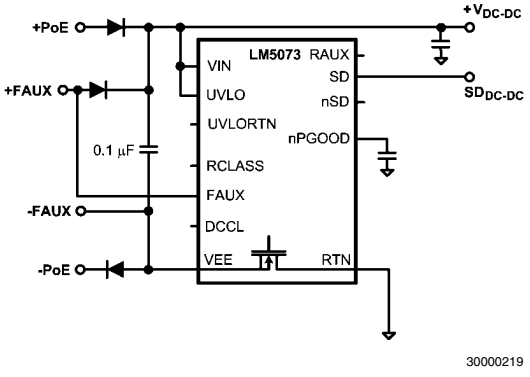


FIGURE 8. The FAUX Configuration

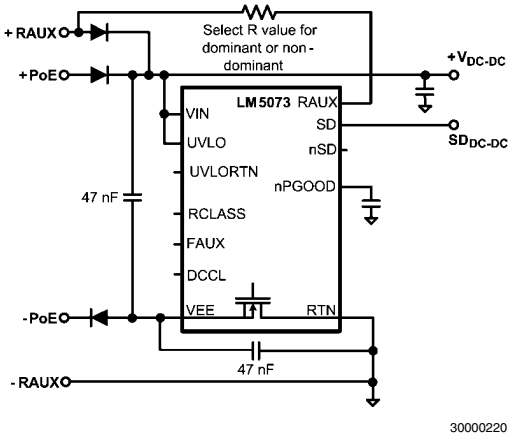


FIGURE 9. The RAUX Configuration

TABLE 3. Comparison Between FAUX and RAUX Operation

Tradeoff	FAUX Operation	RAUX Operation
Hot Swap Protection / Current Limit Protection	Automatically provided by the hot swap MOSFET.	Requires a series resistor to limit the inrush current during hot swap.
Minimum Auxiliary Voltage (at the IC pins)	Limited to 13V by the signature detection mode, or by the power requirement (current limit).	Only limited by 9V minimum input requirement.
Auxiliary Dominance Over PoE	Cannot be forced without external components.	Can be forced with appropriate RAUX pin configuration.
Use of nPGOOD Pin as "Powered from PoE" Indicator	Not applicable as power is delivered through the hot swap interface in both PoE and FAUX modes.	Supported.
Transient Protection	Excellent due to active MOSFET current limit and other voltage protection.	Fair due to passive resistor current limit.

The term "Auxiliary Dominance" mentioned in *Table 3* means that when the auxiliary power source is connected, it will always power the PD regardless of the state of PoE power. "Aux dominance" is achievable only with the RAUX option.

If the PD is not designed for aux dominance, either the FAUX or RAUX power sources will deliver power to the PD only under the following two conditions: (i) If auxiliary power is applied before PoE power, it will prevent the PSE from detecting the PD and will supply power indefinitely. This occurs because the PoE input bridge rectifiers will be reverse biased, and no detection signature will be observed. Under this condition, when the auxiliary supply is removed, power continuity will not be maintained because it will take some time for the PSE to perform signature detection and classification before it will supply power. (ii) If auxiliary power is applied after PoE power is already present and the auxiliary supply voltage is greater than the voltage received from the PSE, then the auxiliary supply will power the PD. Under the second case, if the PSE and auxiliary supply voltages are essentially equal, the load will be shared inversely proportional to the respective output impedances of each supply. (Note: The output impedance of the PSE supply is increased by the cable series resistance).

If PoE power is applied first and has a higher voltage than the non-dominant aux power source, it will continue powering the PD even when the aux power source becomes available. In this case, should PoE power be removed, the auxiliary source will assume power delivery and supply the DC-DC converter loads without interruption.

FAUX Option

With the FAUX option, the LM5073 hot swap MOSFET provides inrush and DC current limit protection for the auxiliary power source. To select the FAUX configuration for an auxiliary voltage lower than nominal PoE voltages, the FAUX pin must be forced above its high threshold to override the UVLO function.

Pulling up the FAUX pin will increase the default DC current limit to 800 mA. This increase in DC current limit is desirable because higher current is required to support the PD output power at the lower input potentials often delivered by auxiliary sources. In cases where the auxiliary supply voltage is comparable to the PoE voltage, there is no need to pull-up the FAUX pin to override UVLO, and the default DC current limit remains at 440 mA. However, if the DC current limit is externally programmed with R_{DCCL}, the condition of the FAUX pin will not affect the programmed DC current limit. In other words, the programmed DC current limit can be considered a "hard limit" that will not vary in any configuration.

RAUX Option

The RAUX option is desirable when the auxiliary supply voltage is significantly lower than the PoE voltage or when aux dominance is desired. The inrush and DC current limits of the LM5073 do not protect or limit the RAUX power source, and an additional resistor in the RAUX input path will be needed to provide transient protection.

To select the RAUX option without aux dominance, simply pull up the RAUX pin to the auxiliary power supply voltage through a high value resistor. Depending on the auxiliary supply voltage, the resistor value should be selected such that the current flowing into the RAUX pin is approximately 100 µA when the pin is mid-way between the lower and upper RAUX thresholds (approximately 4V). For example, with an 18V non-dominant rear auxiliary supply, the pull up resistor should be:

$$\frac{V_{AUX} - V_{RAUX}}{100\ \mu A} - \frac{18V - 4V}{100\ \mu A} = 140\ k\Omega$$

If the PSE load capacity is limited and insufficient, aux dominance will be a desired feature to off-load PoE power for other PDs that do not have auxiliary power available. Aux dominance is achieved by pulling the RAUX pin up to the auxiliary supply voltage through a lower value (~5 kΩ) resistor that delivers at least 330 µA into the RAUX pin. When this higher RAUX current level is detected, the LM5073 shuts down the PD interface. In aux dominant mode, the auxiliary power source will supply the PD as soon as it is applied. PD operation will not be interrupted when the aux power source is connected. The PoE source may or may not actually be removed by the PSE, although the DC current from the network cable is effectively reduced to zero (<150 µA). IEEE 802.3af requires the AC input impedance to be greater than 2 MΩ to ensure PoE power removal. This condition is not satisfied when the auxiliary power source is applied. The PSE may remove power from a port based on the reduction in DC current. This is commonly known as DC Maintain Power Signature (DC MPS), a common feature in many PSE systems.

When using the RAUX configuration, the hot swap MOSFET may become disabled which will cause a high impedance at the VEE pin. To provide a high frequency, low impedance

path for the IC's substrate current from VEE to RTN, the 0.1 µF signature capacitor is split equally between VIN to VEE, and VEE to RTN, as shown in *Figure 9*. The two capacitors are effectively connected in parallel. This will not affect signature mode, and can be used for all configurations.

It should be noted that rear auxiliary non-dominance does not imply PoE dominance. PoE dominance requires a different circuit configuration if continuity of power is desired. Please contact National Semiconductor for support on PoE dominant solutions.

A Note About FAUX and RAUX Pin False Input State Detection

The FAUX and RAUX pins are used to sense the presence of auxiliary power sources. The input voltage of each pin must remain low when the auxiliary power sources are absent. However, the Or-ing diodes feeding the auxiliary power are not ideal and exhibit reverse leakage current that can flow from the PoE input to both the FAUX and RAUX pins. When PoE power is applied, these leakage currents may elevate the potentials of the FAUX and RAUX pins to false logic states.

A failure mode may be observed when the power diode feeding the front auxiliary input leaks excessively. The leakage current may elevate the voltage on the FAUX pin above the FAUX input threshold, which will force UVLO release. This would certainly interrupt any attempt by the LM5073 PD interface to perform the signature or classification functions.

When the power diode that feeds the rear auxiliary input leaks, the false signal could imply a rear auxiliary supply is present. In this case, the internal hot swap MOSFET will be turned off. This would block PoE power flow and prevent startup.

This leakage problem at the control input pins can be easily solved. As shown in *Figure 9*, an additional pull-down resistor (Rpd) across each auxiliary power control input provides a path for the diode leakage current so that it will not create false states on the FAUX or RAUX pins.

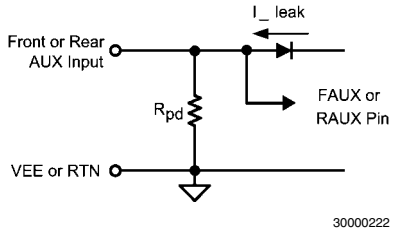


FIGURE 10. Bypassing Resistor – Prevents False FAUX and RAUX Pin Signaling

Thermal Protection

The LM5073 includes internal thermal shutdown circuitry to protect the IC in the event the maximum junction temperature is exceeded. This circuit prevents catastrophic overheating due to accidental overload of the hot swap MOSFET or other circuitry. Typically, thermal shutdown is activated at 165°C, causing the hot swap MOSFET and classification regulator to be disabled. The DC-DC converter control outputs will be disabled after the power good timer has expired. The thermal protection is non-latching, therefore after the temperature drops by the 20°C nominal hysteresis, the hot swap MOSFET is re-activated. If the cause of overheating has not been eliminated, the circuit will oscillate in and out of the thermal shutdown mode.

Application Examples

The following are a few application examples. *Figure 11* shows the typical LM5073 PD interface fully compliant to IEEE802.3af.

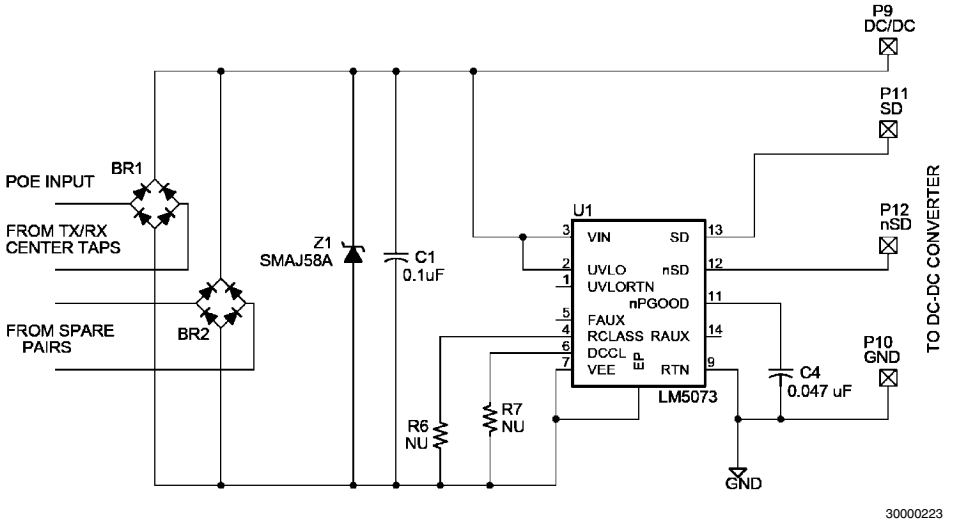


FIGURE 11. Typical LM5073 PoE PDI

Figure 12 shows the LM5073 PD interface supporting front auxiliary power configuration. According to particular application requirements, users can select an appropriate DC-DC converter to optimize the PD design. National's LM5025/26 active clamp forward converter evaluation board is recommended for a high efficiency, isolated application; the LM5020 flyback converter evaluation board for a low cost, isolated application; and the LM5005 or LM5576 buck regulator evaluation boards for low cost, non-isolated design.

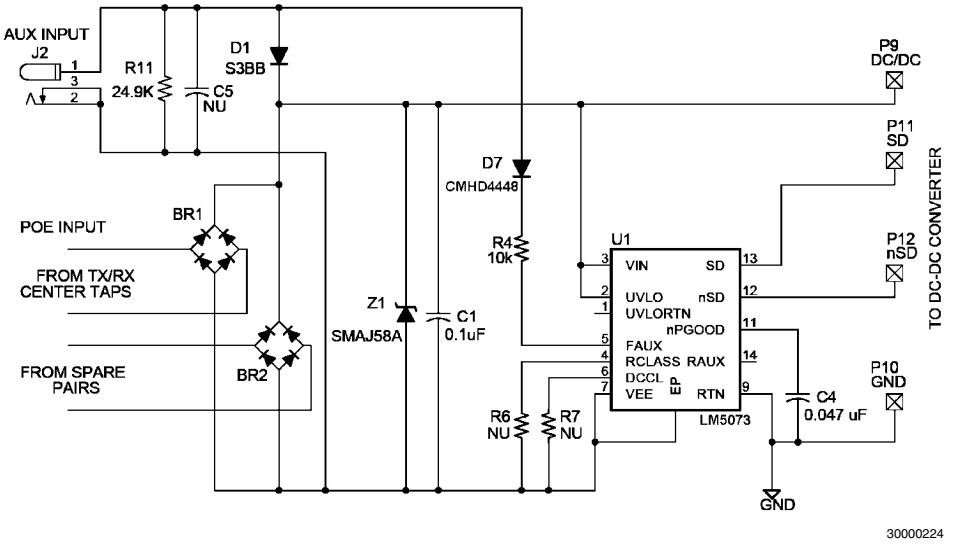


FIGURE 12. LM5073 PoE PDI with Front Auxiliary Power Support

Figure 13 shows the LM5073 PD interface supporting rear auxiliary power configuration. Similarly, users can select a DC-DC converter to optimize the PD design. National's LM5025/26 active clamp forward converter evaluation board is recommended for a high efficiency, isolated application; the LM5020 flyback converter evaluation board for a low cost, isolated application; and the LM5005/5567 buck regulator evaluation board for a low cost, non-isolated design.

Additional features are included.

1. The optional common-mode and differential mode input filters are added to reduce the conducted emissions below most applicable standards.
2. Two options for RAUX inrush limiting are offered, selectable with JMP2. Two resistors R1 and R2 form a low cost solution, or a MOSFET limiter for a high performance solution.
3. Aux dominant is selectable by shorting JMP1. With JMP1 open, the circuit is not in aux dominant mode.
4. An optional LED1 indicates the PoE operating mode and it is enabled by connecting JMP7.

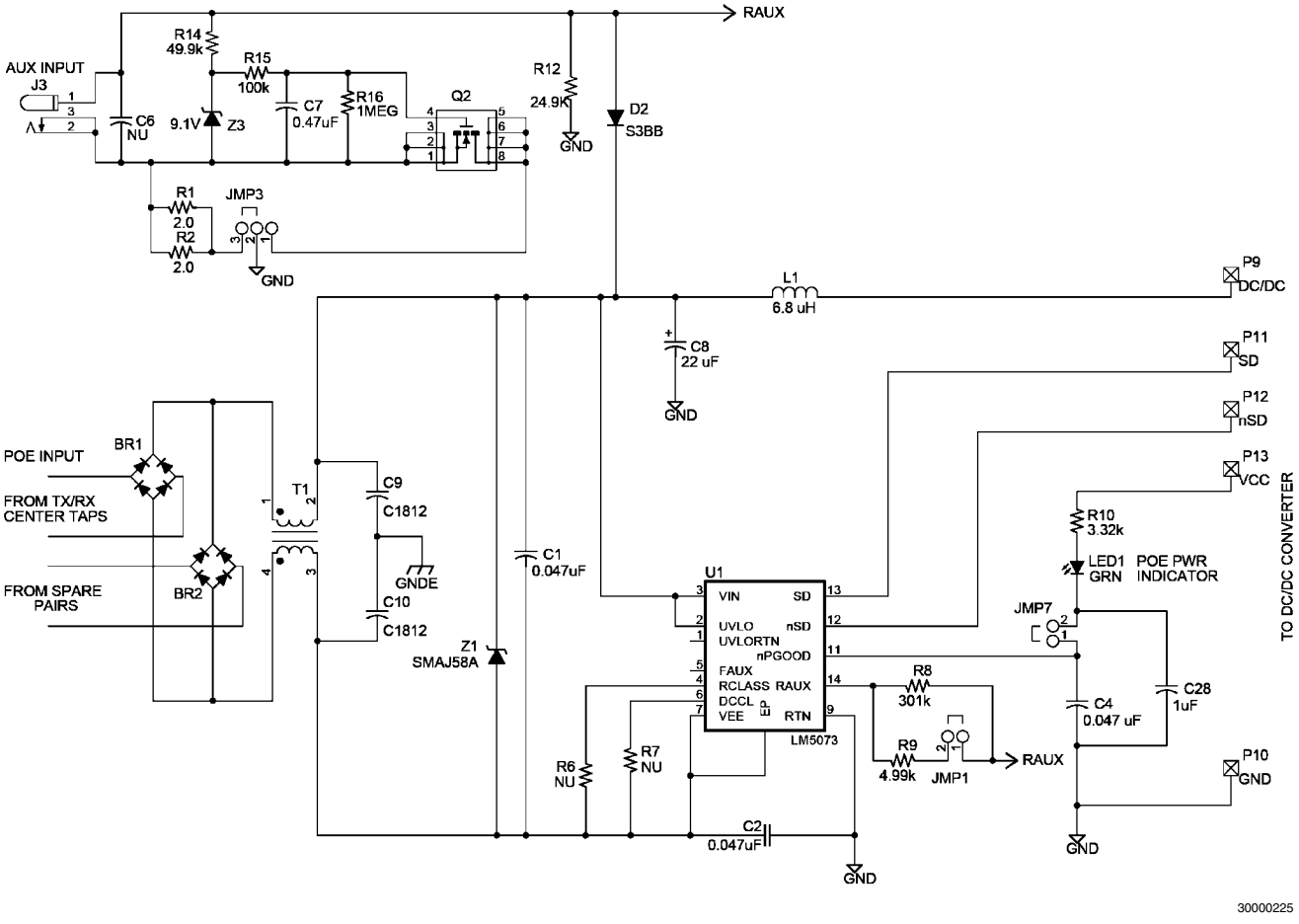


FIGURE 13. LM5073 PoE PDI with Rear Auxiliary Power Support

Figure 14 shows an example of LM5073 PD interface and LM5576 buck regulator for a low cost, non-isolated application.

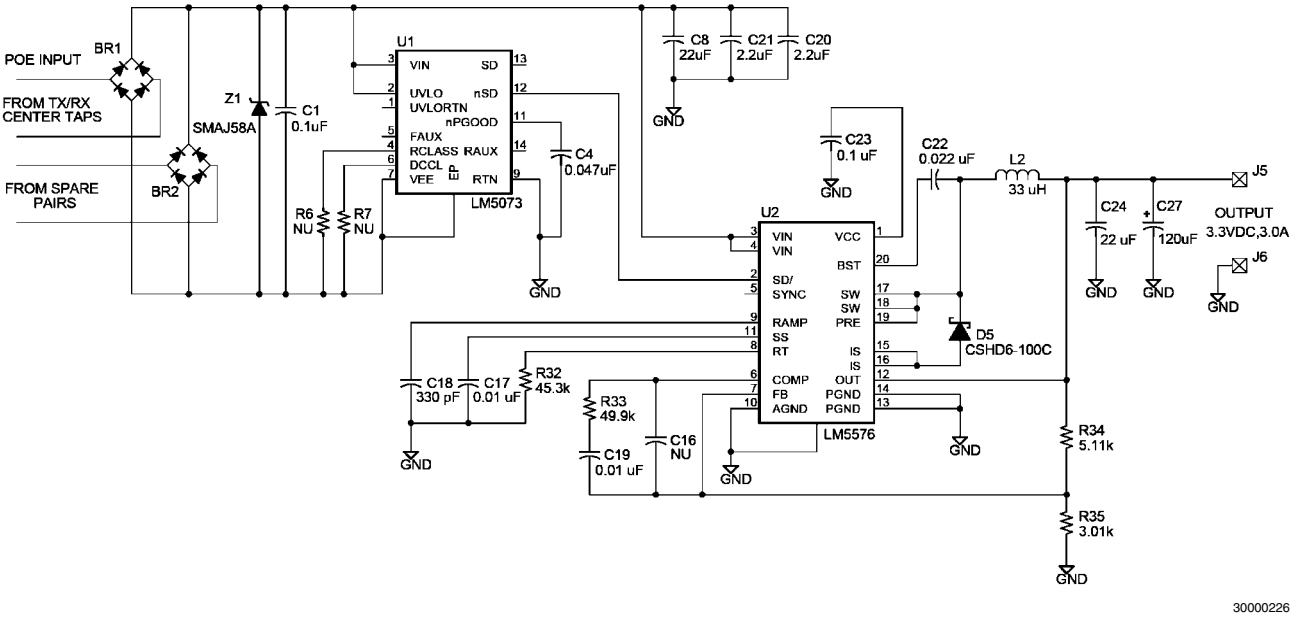
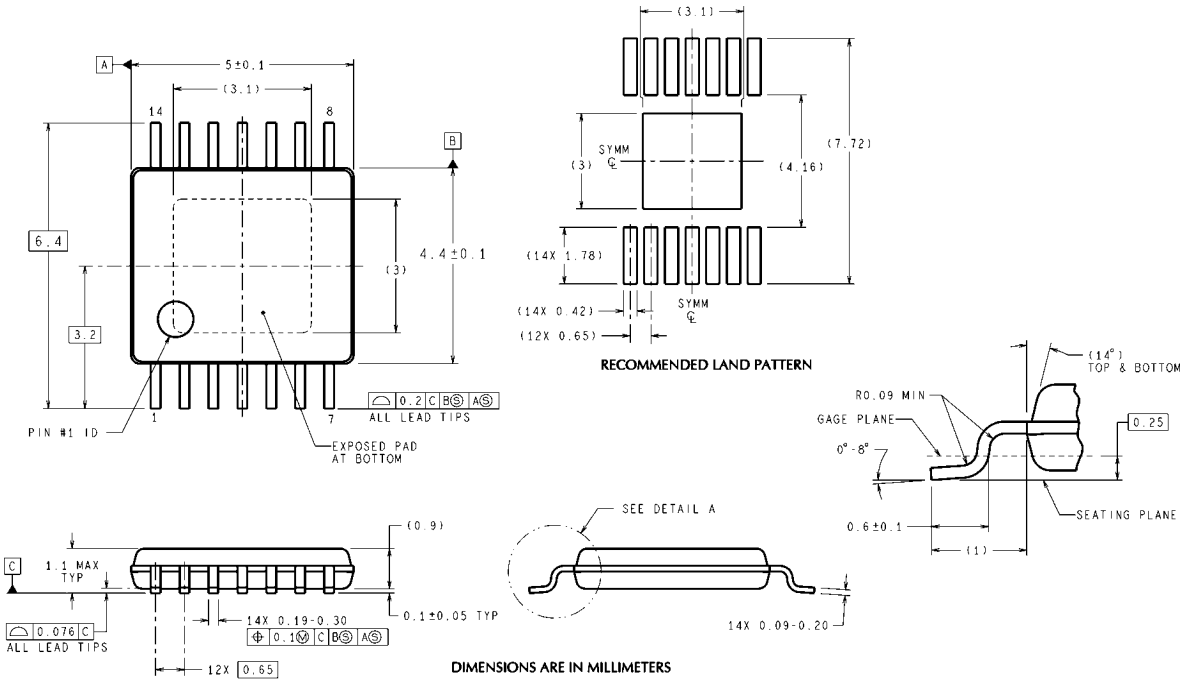


FIGURE 14. LM5073 in Isolated PD Design with LM5576 Buck Regulator

Physical Dimensions inches (millimeters) unless otherwise noted



MXA14A (Rev A)

14 Lead TSSOP-EP
NS Package Number MXA14A

Notes

Notes

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